What is claimed is:

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- 1. A ferroelectric register, comprising:
- a pull-up switch for outputting a power voltage when a pull-up enable signal is activated;
 - a pull-up driving unit for receiving the power voltage from the pull-up switch, and for pulling up a voltage of a data storage node to the power voltage;
- a write enable control unit for transmitting a 10 differential data to the data storage node according to a write control signal;
 - a ferroelectric capacitor unit including at least two ferroelectric capacitors connected in parallel between the data storage node and a plate line, and storing the differential data when a cell plate signal is activated;
 - a pull-down switch for transmitting a ground voltage to the data storage node when a pull-down enable signal is activated; and
- a pull-down driving unit for receiving the ground voltage from the pull-down switch, and for pulling down the voltage of the data storage node to the ground voltage.
 - 2. The ferroelectric register of claim 1, wherein, in the ferroelectric capacitor unit, at least two ferroelectric capacitors share the same ferroelectric layer on the same

plane.

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- 3. The ferroelectric register of claim 1, wherein, in the ferroelectric capacitor unit, at least two ferroelectric capacitors are formed by stacking ferroelectric layers symmetrically upon and beneath a common electrode layer.
- 4. The ferroelectric register of claim 1, wherein, in the ferroelectric capacitor unit, at least two ferroelectric capacitors are connected in parallel between the data storage node and the ground voltage.
 - 5. The ferroelectric register of claim 1, further comprising a cell plate voltage control unit for pumping the cell plate signal from a power voltage level to a pumping voltage level according to a cell plate control signal and a power voltage control signal.
- 6. The ferroelectric register of claim 5, wherein the cell plate voltage control unit comprises:
 - a delay unit for outputting a delay signal by delaying the cell plate control signal for a predetermined time;
 - a pumping unit for outputting a pumping signal by pumping the power voltage to a pumping voltage level according to the delay signal, when receiving the power

voltage control signal; and

a level control unit for outputting the pumped cell plate signal by level-shifting the pumping signal and the cell plate control signal.

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7. The ferroelectric register of claim 5, wherein, in the ferroelectric capacitor unit, at least two ferroelectric capacitors are connected in parallel between the data storage node and the ground voltage.

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8. The ferroelectric register of claim 5, wherein, in the ferroelectric capacitor unit, at least two ferroelectric capacitors share the same ferroelectric layer on the same plane.

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9. The ferroelectric register of claim 5, wherein, in the ferroelectric capacitor unit, at least two ferroelectric capacitors are stacked symmetrically upon and beneath a common electrode layer.

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- 10. A method for manufacturing a capacitor of a ferroelectric register, comprising:
- a first process for forming at least two bottom electrode layers commonly connected to an output terminal of the register;

- a second process for forming a ferroelectric layer commonly corresponding to at least two bottom electrode layers on the two bottom electrode layers; and
- a third process for forming a top metal layer receiving a cell plate signal and commonly corresponding to at least two bottom electrode layers on the ferroelectric layer.
- 11. A method for manufacturing a capacitor of a 10 ferroelectric register, comprising:
 - a first process for forming a contact plug on a bit line;
 - a second process for sequentially stacking a first electrode layer, a first ferroelectric layer, a second electrode layer, a second ferroelectric layer and a third electrode layer on the contact plug;

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- a third process for forming an insulation film on the third electrode layer;
- a fourth process for forming a first contact hole for opening a predetermined area of the bit line and a second contact hole for opening a predetermined area of the third electrode layer on the insulation film; and
 - a fifth process for electrically connecting the bit line to the third electrode layer by performing a metal process on the resulting structure on which the first and

second contact holes have been formed.